# 21555 Bridge Reference Design

## Schematics

***December 2000***

Order Number: 278364-001

# DE1B55501 Schematic Directory

| SHEET | DESCRIPTION |
|---|---|
| sht 1 | Schematic Directory |
| sht 2 | Block diagram |
| sht 3 | 21555 (DrawBridge - 66MHz) |
| sht 4 | 21555 Parallel & Serial ROM, latches and MDM |
| sht 5 | Secondary clock generation & hot swap test |
| sht 6 | Pull up resistors for 21555 signals |
| sht 7 | Primary Edge Connector and svio generation |
| sht 8 | System Slot - PICMG or PCI Option |
| sht 9 | PCI Secondary Option slots Middle and Bottom |
| sht 10 | 3.3V Voltage regulator and bulk decoupling |
| sht 11 | Mictor Connectors |

REVISION

CHK | CHANGE NO. | REV

EB555 21555 EVALUATION BOARD

Intel

DRN. | DATE

CHK'D. | DATE

ENG. GWRD | DATE

BOARD LOCATION:

SHEET | OF

USRA:

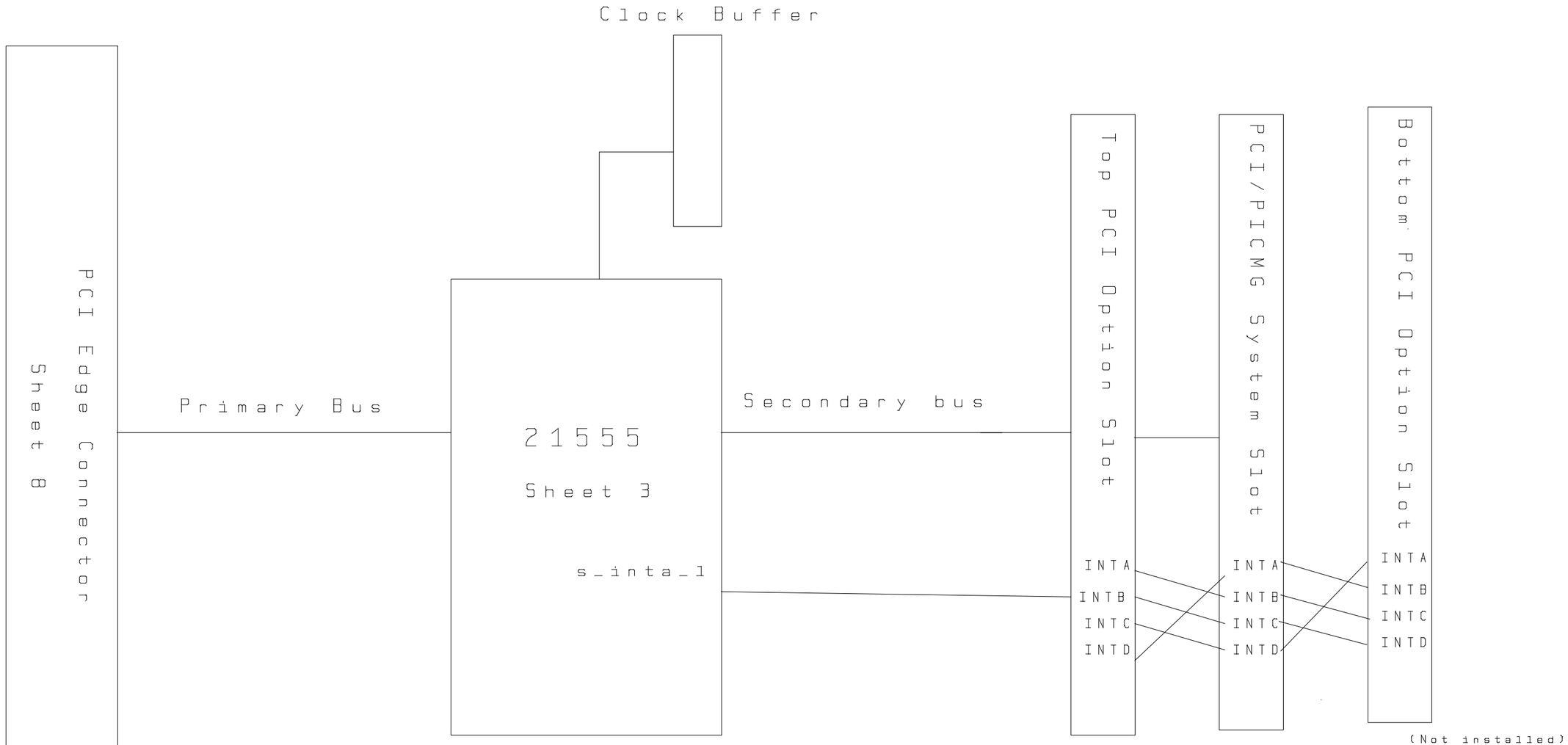
FIRST USED ON OPTION/MODEL:

TOP DOCUMENT NUMBER:

TITLE: DE1B55501

SIZE B | CODE | NUMBER | REV.

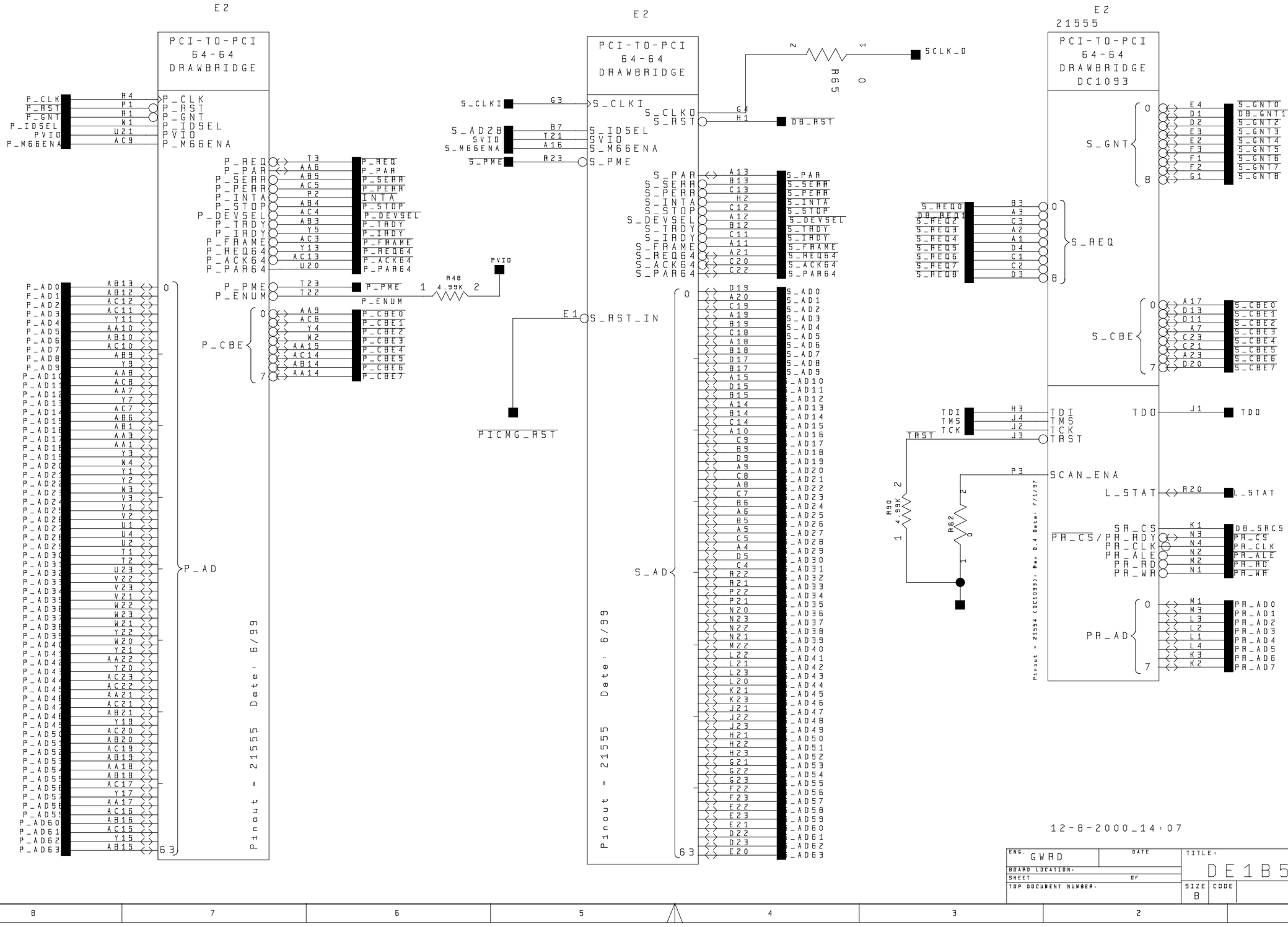
# EB555 Block Diagram



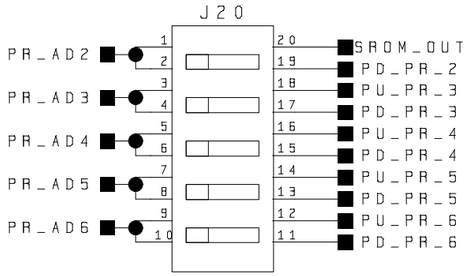

| REVISION | | |
|---|---|---|
| CHK | CHANGE NO. | REV |

Intel

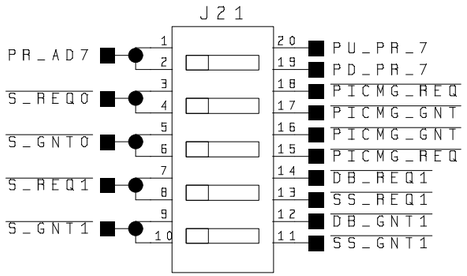
| | | | | | |
|---|---|---|---|---|---|
| DRN. | DATE | ENG. | DATE | TITLE: DE1B55501 | |
| CHK'D. | DATE | BOARD LOCATION: | | | |
| USRA: | | SHEET | OF | | |
| FIRST USED ON OPTION/MODEL: | | TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER | REV. 2 |


E2
PCI-TO-PCI
64-64
DRAWBRIDGE
P_CLK
P_RST
P_GNT
P_IDSEL
PVIO
P_M66ENA
P_REQ
P_PAR
P_SERR
P_PERR
P_INTA
P_STOP
P_DEVSEL
P_TRDY
P_IRDY
P_FRAME
P_REQ64
P_ACK64
P_PAR64
P_PME
P_ENUM
P_CBE
P_AD
P_AD63
R48
4.99K
PVIO
Pinout = 21555 Date: 6/99
E2
PCI-TO-PCI
64-64
DRAWBRIDGE
S_CLKI
S_AD28
S_M66ENA
S_PME
S_CLKO
S_RST
S_IDSEL
SVIO
S_PAR
S_SERR
S_PERR
S_INTA
S_STOP
S_DEVSEL
S_TRDY
S_IRDY
S_FRAME
S_REQ64
S_ACK64
S_PAR64
S_RST_IN
S_AD
S_AD63
R65
0
SCLK_D
DB_RST
PICMG_RST
Pinout = 21555 Date: 6/99
E2
21555
PCI-TO-PCI
64-64
DRAWBRIDGE
DC1093
S_GNT
S_REQ
S_CBE
TDI
TMS
TCK
TRST
TDO
SCAN_ENA
L_STAT
PR_CS/
PR_RD
PR_CLK
PR_ALE
PR_RD
PR_WR
PR_AD
R90
4.99K
R62
0
DB_SRC5
PR_CS
PR_CLK
PR_ALE
PR_RD
PR_WR
PR_AD0
PR_AD1
PR_AD2
PR_AD3
PR_AD4
PR_AD5
PR_AD6
PR_AD7
Pinout = 21554 (DC1093); Rev 0.4 Date: 7/1/97
12-8-2000_14:07
ENG. GWRD
DATE
TITLE: DE1B55501
BOARD LOCATION:
SHEET OF
TOP DOCUMENT NUMBER:
SIZE B
CODE
NUMBER
REV. 3

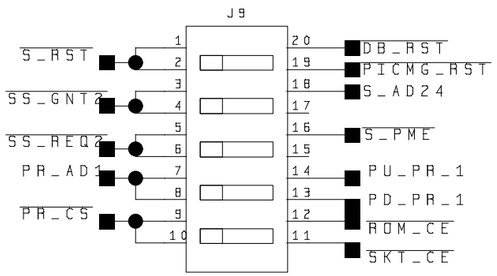
## Initialization Selections



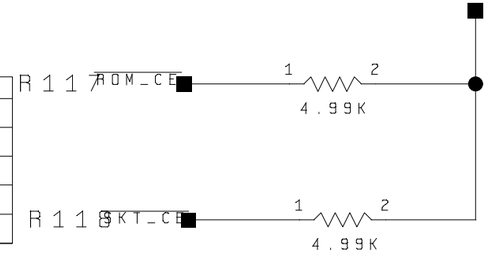

| J20 | *DOWN = Pull DOWN* | *UP = Pull UP* |
|---|---|---|
| SW1 = pr_2 | NO SROM | SROM |
| SW2 = pr_3 | DEBUG – No Lockout | NORMAL – Lockout |
| SW3 = pr_4 | Synch | Async |
| SW4 = pr_5 | DB S_CLK_0 DISABLED | DB S_CLK_0 ENABLED |
| SW5 = pr_6 | 21554 as Central Function | System Slot as Central Function |



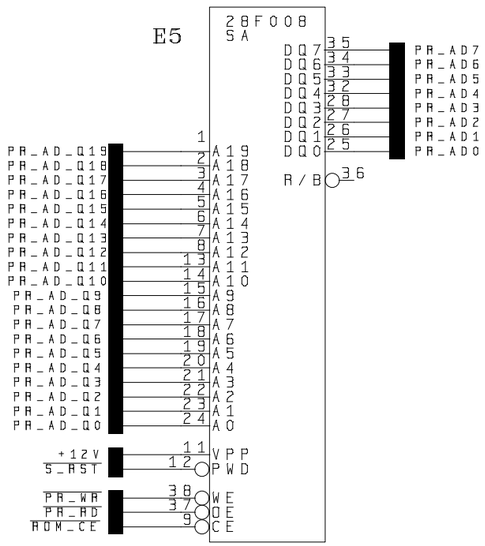

| J21 . . . | SYSTEM SLOT AS ARBITER | DRAWBRIDGE AS ARBITER |
|---|---|---|
| SW1=pr_ad7 | *DOWN* | *UP* |
| SW2=DB(s_req0) | *DOWN* | *UP* |
| SW3=DB(s_gnt0) | *DOWN* | *UP* |
| SW4=s_req1 | *DOWN* | *UP* |
| SW5=s_gnt1 | *DOWN* | *UP* |

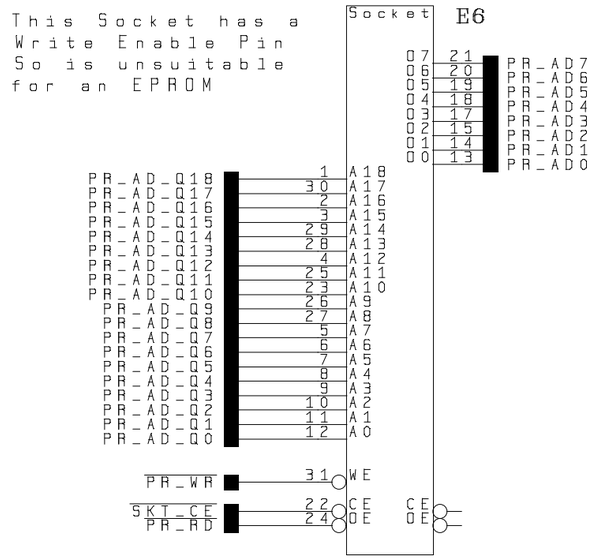



| J9 | *DOWN = Pull DOWN* | *UP = Pull UP* |
|---|---|---|
| SW1 = s_rst | PICMG_RST | DB_RST |
| SW2 = IDSEL | PICMG (top slot) | PCI (top slot) |
| SW3 = pr_4 | PICMG (top slot) | PCI (top slot) |
| SW4 = pr_5 | Enable Prim 64–bit | Disable Prim 64–bit |
| SW5 = pr_6 | ROM Socket | Flash ROM |

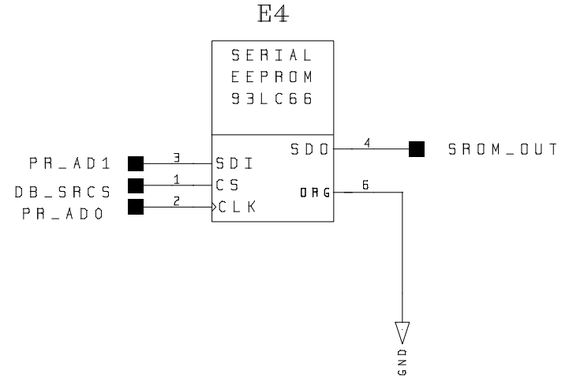



## Parallel ROM

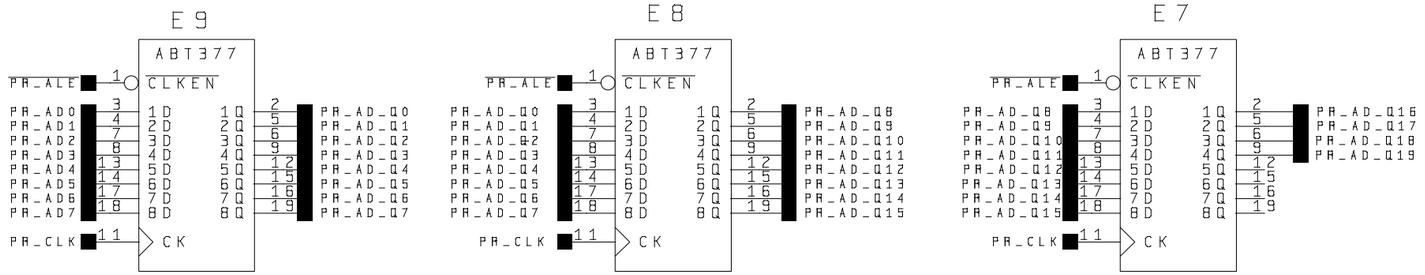



## Serial ROM




## Parallel ROM Address Latches

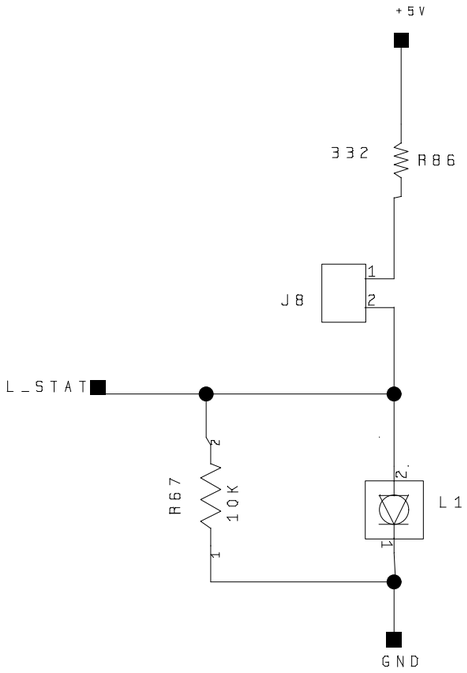


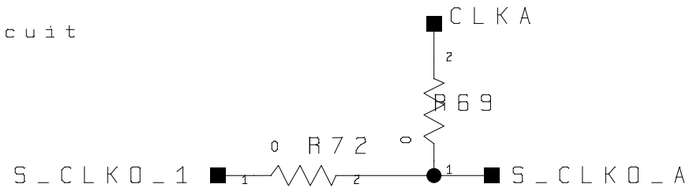

| REVISION | | |
|---|---|---|
| CHK | CHANGE NO. | REV |

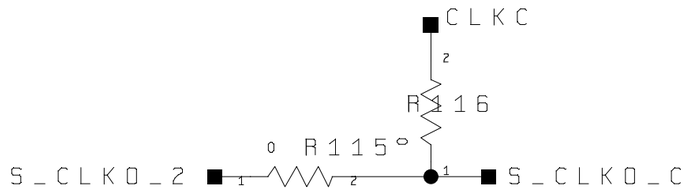
Intel

| | | | | |
|---|---|---|---|---|
| DRN. | DATE | ENG. | DATE | TITLE: DE1B55501 |
| CHK'D. | DATE | BOARD LOCATION: | | |
| USRA: | | SHEET | OF | |
| FIRST USED ON OPTION/MODEL: | | TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER / REV: 4 |

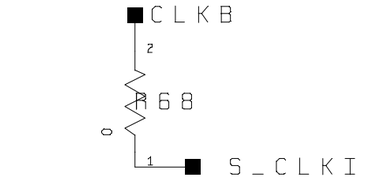
# Compact PCI Hot Swap Test Circuit

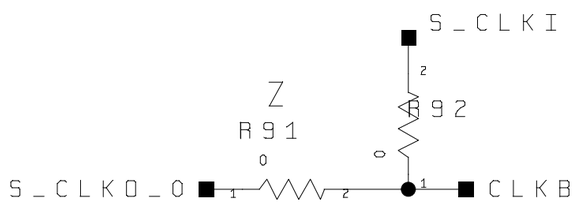



Postional requirement



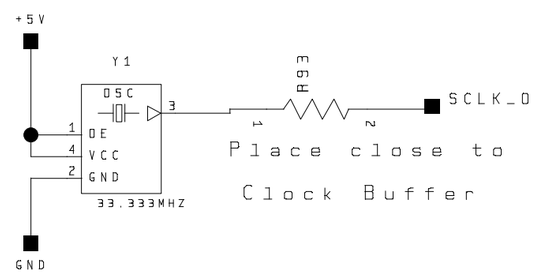



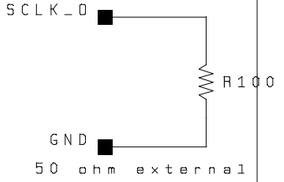

| Central Function | | | |
|---|---|---|---|
| 21554 | | System Slot | |
| In | Out | In | Out |
| R65 | R68 | R68 | R65 |
| R72 | R69 | R69 | R72 |
| R91 | R92 | R92 | R73 |
| R115 | R116 | R116 | R91 |
| | | | R115 |

| External Oscillator | |
|---|---|
| In | Out |
| R93 | R65 |

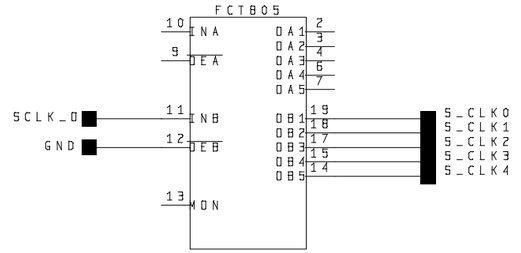
## Clock Generation

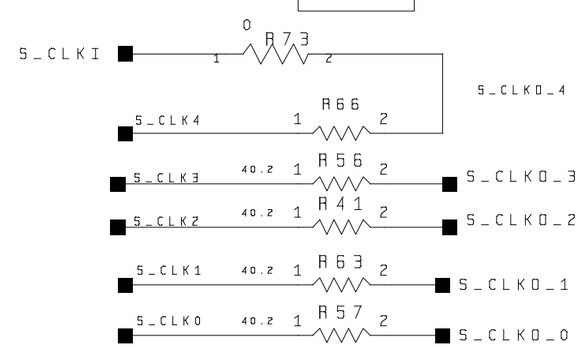
No Connection




E3




Series resistors should be close to the buffer outputs.
Clock traces should be kept the same length
Keep clock signals on same layer
Avoid vias and other transmission discontinuities

| REVISION | | |
|---|---|---|
| CHK | CHANGE NO. | REV |

Intel

DRN. DATE ENG. DATE

CHK'D. DATE

BOARD LOCATION:

SHEET OF

USRA:

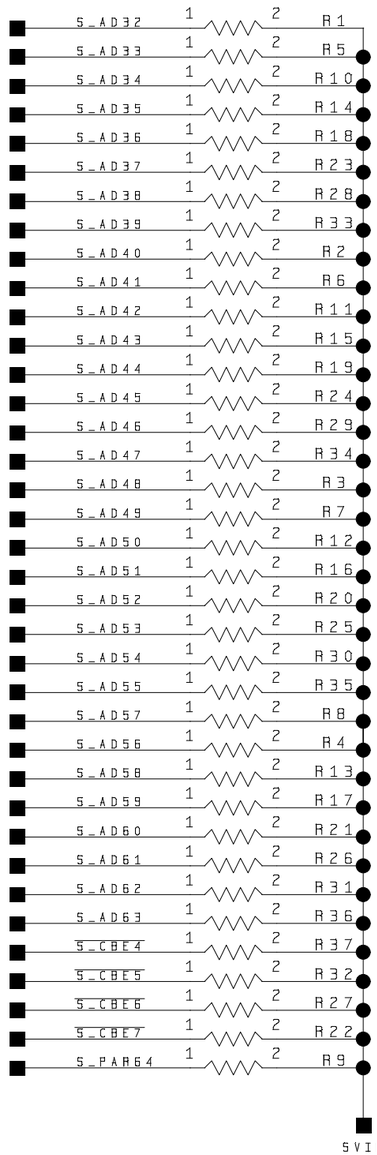
FIRST USED ON OPTION/MODEL:

TOP DOCUMENT NUMBER:

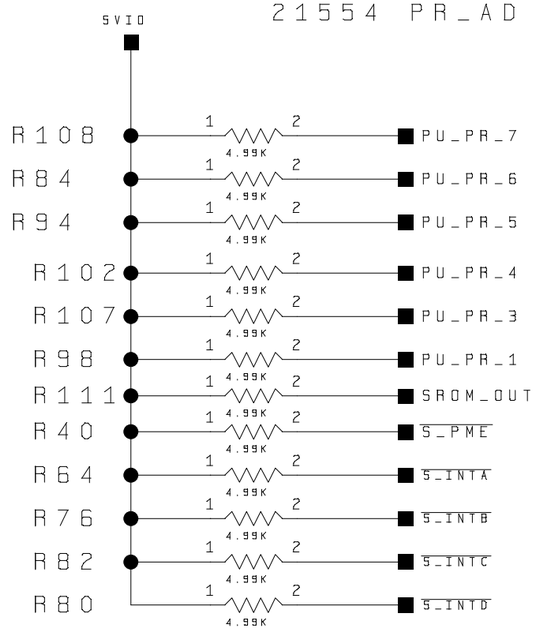
TITLE: DE1B55501

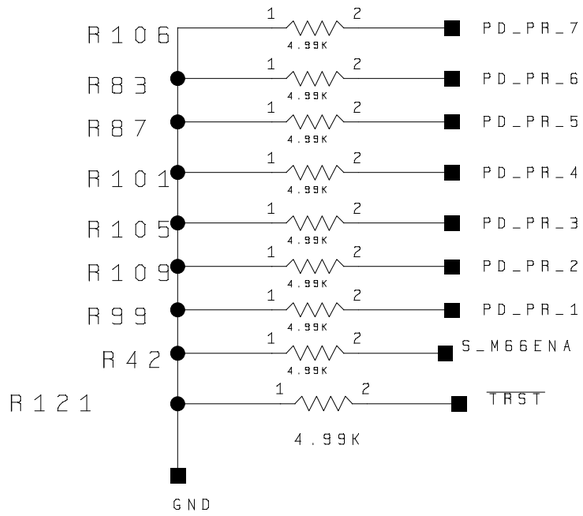
SIZE B | CODE | NUMBER | REV. 5

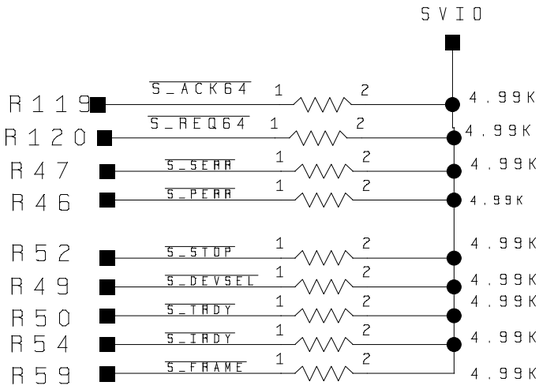
## 64-Bit Pull-Ups
R = 4.99K ohms

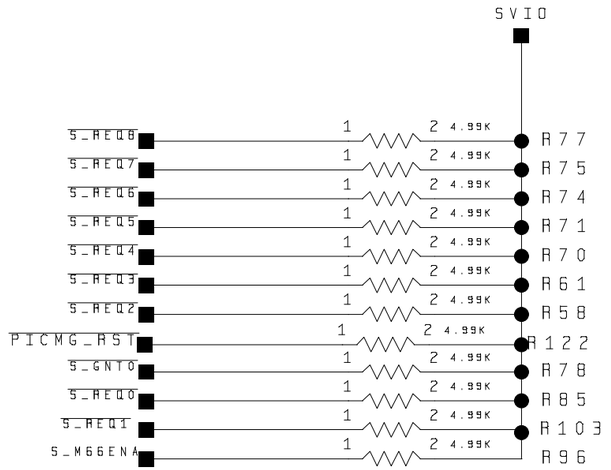



## 21554 PR_AD and Misc Pull-Ups/Downs




| REVISION | | |
|---|---|---|
| CHK | CHANGE NO. | REV |

Intel

| | | | | | |
|---|---|---|---|---|---|
| DRN. | DATE | ENG. | DATE | TITLE: DE1B55501 | |
| CHK'D. | DATE | BOARD LOCATION: | | | |
| USRA: | | SHEET | OF | | |
| FIRST USED ON OPTION/MODEL: | | TOP DOCUMENT NUMBER: | | SIZE B | CODE | NUMBER | REV. C |

21-PCI64-00

PCI_U_64

J3

Edge Connector

Primary PCI Bus

NOTE: PRSNT1 Grounded

NOTE: R43, R45, and R114 are not populated as they are the responsibility of the motherboard.

P_PME Input

N-CHAN MOSFET

Q1

svio generation ckt

SVIO

R97

R95

0.22UF C78 C61 C10 C79

Place 1 0.22uf Cap close to each of the Connectors on Pages 9, 10, & 11

Place this capacitor near pin B19 of connector this page.

C76 0.22UF

R45 4.99K

R88

R43 4.99K

C48 C68 C58 C56 C47 C34 C23 C24 0.1UF .022UF .01UF

C52 C72 C36

P_LOCK

P_ACK64

P_REQ64

P_M66ENA

KEYWAY

KEY

RESERVED

PVIO

GND

+5V

+3V

+12V

-12V

TCK

TMS

TDI

TDO

INTA

INTB

INTC

INTD

P_RST

P_GNT

P_CLK

P_REQ

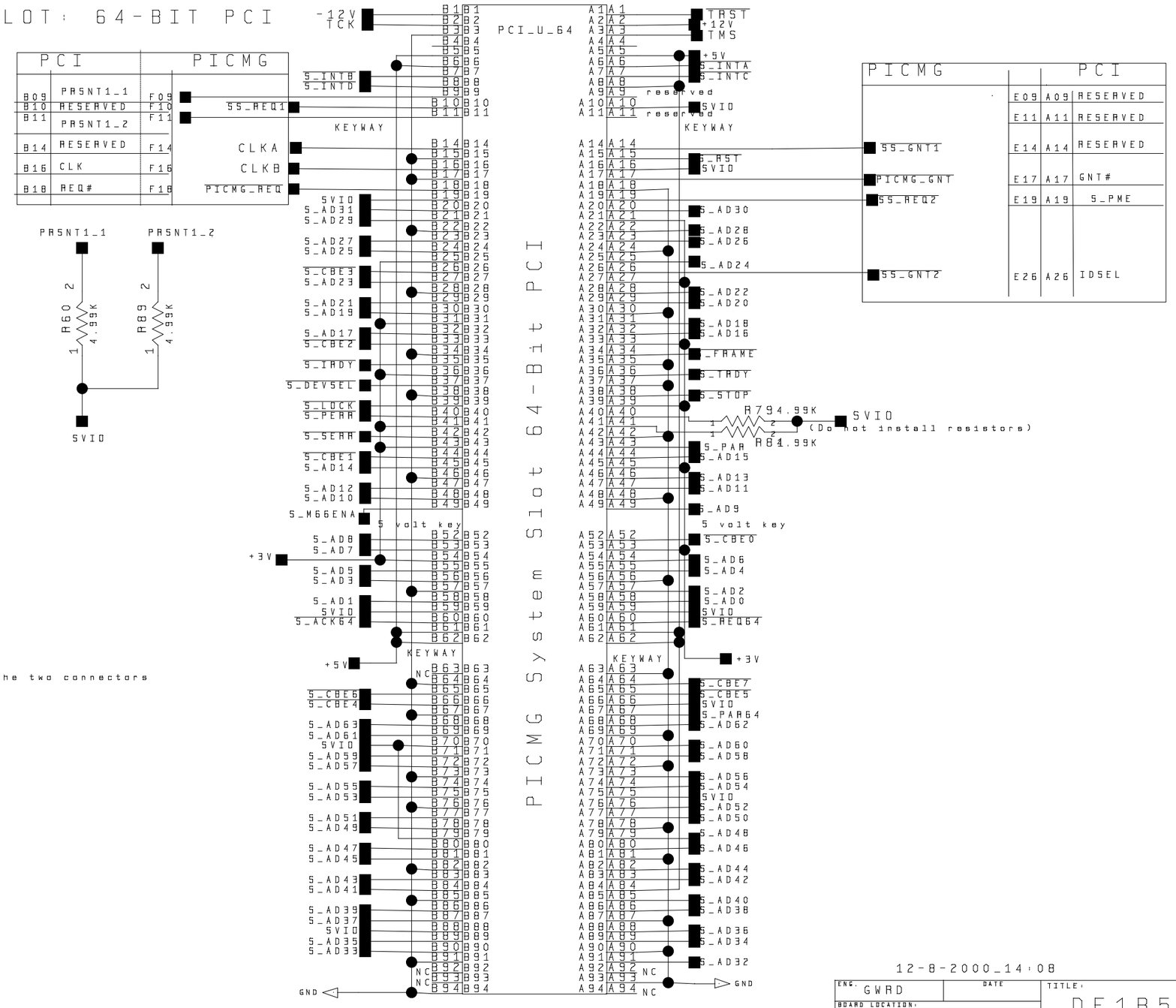
P_AD31 P_AD29 P_AD27 P_AD25 P_CBE3 P_AD23 P_AD21 P_AD19 P_AD17 P_CBE2 P_IRDY P_DEVSEL P_PERR P_SERR P_CBE1 P_AD14 P_AD12 P_AD10 P_AD8 P_AD7 P_AD5 P_AD3 P_AD1 P_CBE6 P_CBE4 P_AD63 P_AD61 P_AD59 P_AD57 P_AD55 P_AD53 P_AD51 P_AD49 P_AD47 P_AD45 P_AD43 P_AD41 P_AD39 P_AD37 P_AD35 P_AD33

P_AD30 P_AD28 P_AD26 P_AD24 P_IDSEL P_AD22 P_AD20 P_AD18 P_AD16 P_FRAME P_TRDY P_STOP P_PAR P_AD15 P_AD13 P_AD11 P_AD9 P_CBE0 P_AD6 P_AD4 P_AD2 P_AD0 P_CBE7 P_CBE5 P_PAR64 P_AD62 P_AD60 P_AD58 P_AD56 P_AD54 P_AD52 P_AD50 P_AD48 P_AD46 P_AD44 P_AD42 P_AD40 P_AD38 P_AD36 P_AD34 P_AD32

| | | | |
|---|---|---|---|
| ENG. GWRD | DATE | TITLE: DE1B555501 | |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER | REV. |

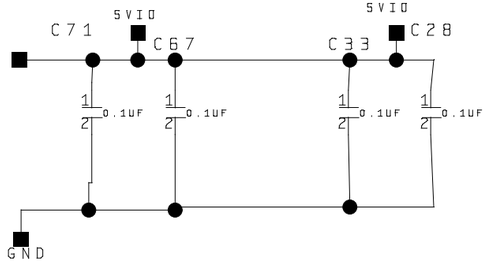
# SYSTEM SLOT: 64-BIT PCI

J101
12-39839-19



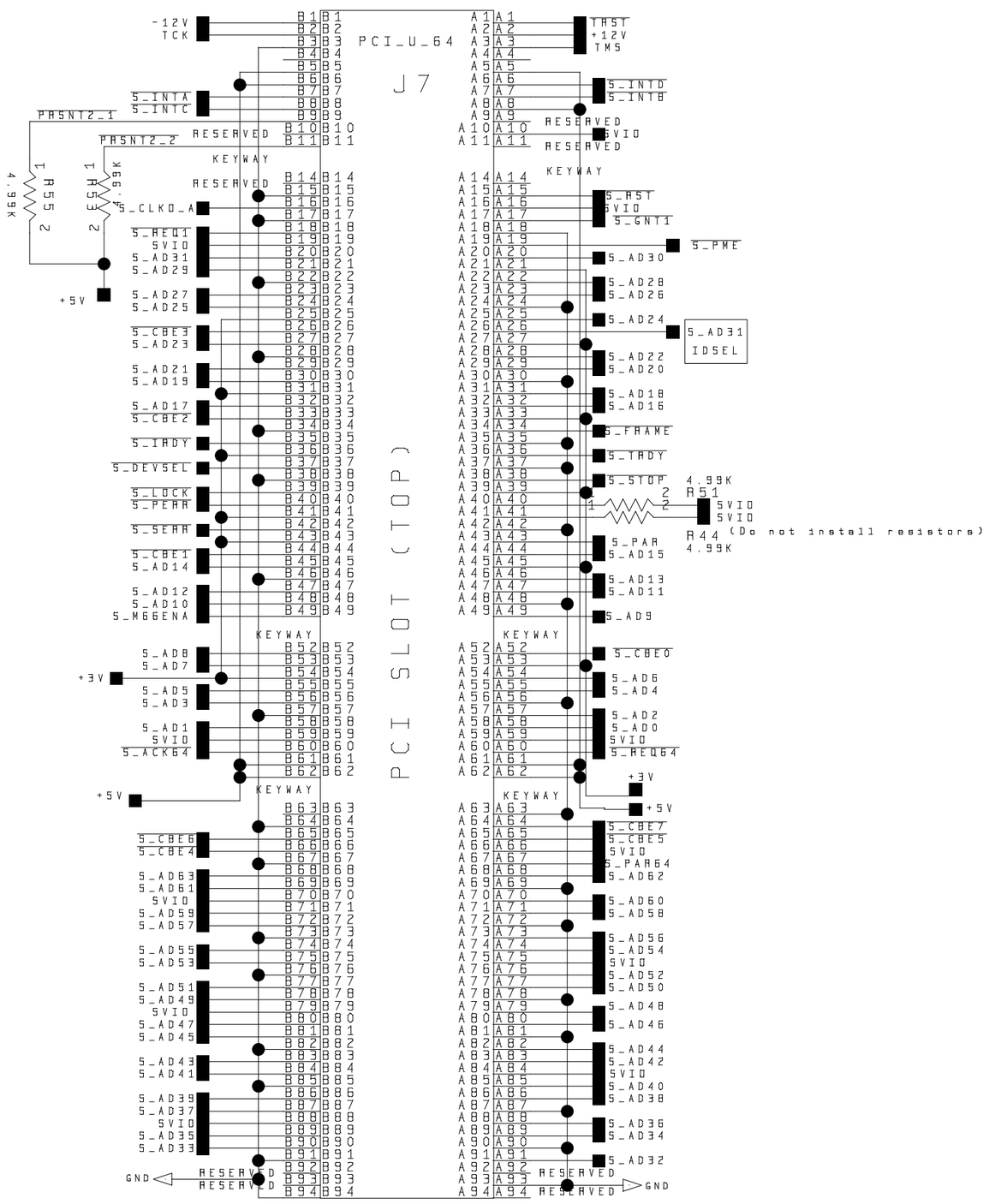

| PCI | | PICMG |
|---|---|---|
| B09 | PRSNT1_1 | F09 |
| B10 | RESERVED | F10 |
| B11 | PRSNT1_2 | F11 |
| B14 | RESERVED | F14 |
| B16 | CLK | F16 |
| B18 | REQ# | F18 |

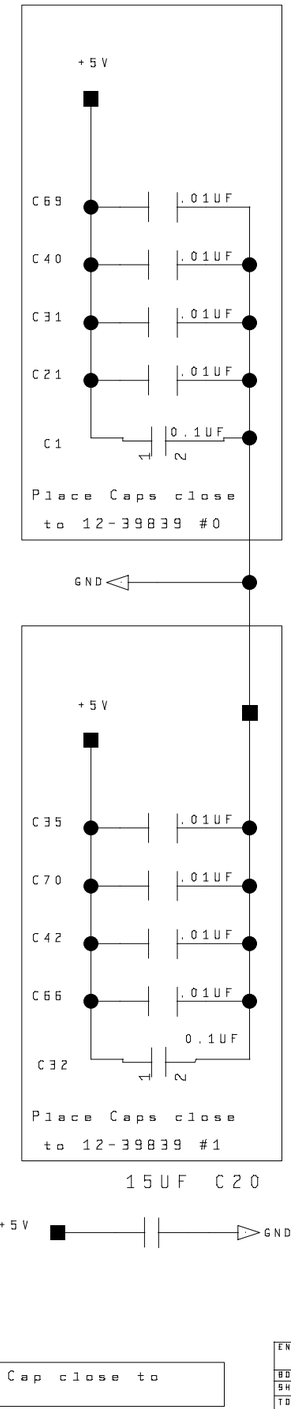
Put two 0.1uF and two 0.22uF close to each of the two connectors




12-8-2000_14:08

| | | |
|---|---|---|
| ENG. GWRD | DATE | TITLE: DE1B555501 |
| BOARD LOCATION: | | |
| SHEET | OF | |
| TOP DOCUMENT NUMBER: | SIZE B / CODE / NUMBER | REV. 03 |



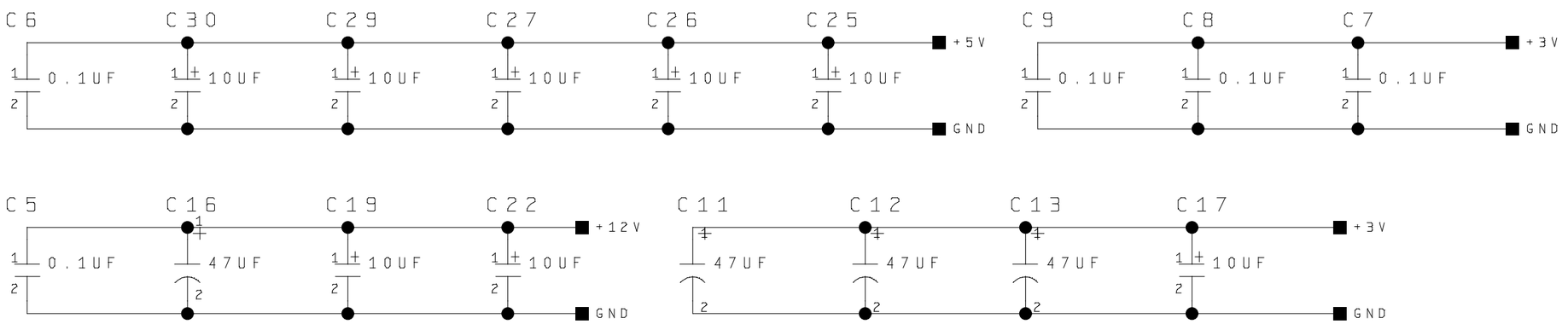



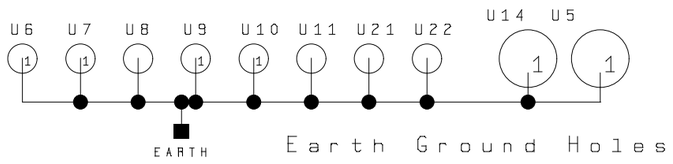

Mount 15uf Cap close to card edge

12-8-2000_14:08

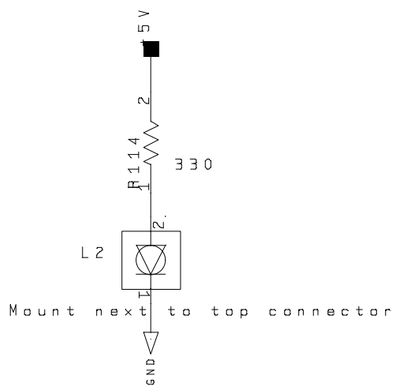
| | | | |
|---|---|---|---|
| ENG. GWRD | DATE | TITLE: DE1B555501 | |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER | REV. 9 |

## Decoupling; bulk, for all power planes



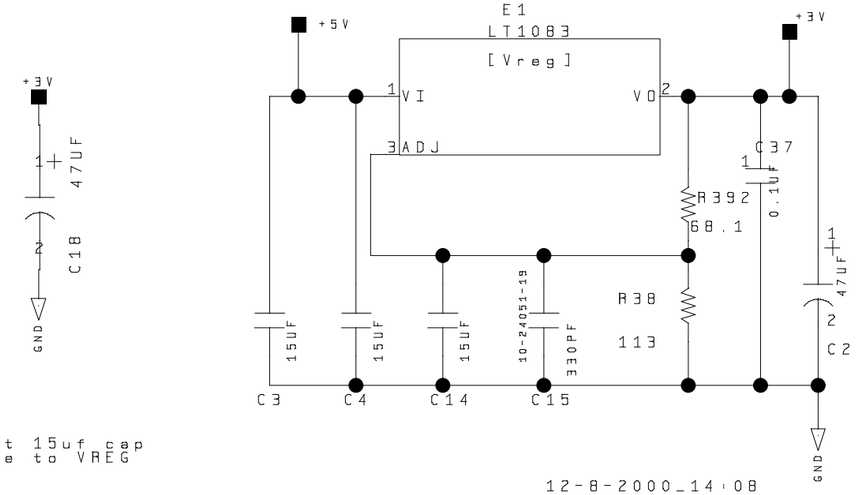




Earth Ground Holes




Mount next to top connector

## Power regulation (3.3V)



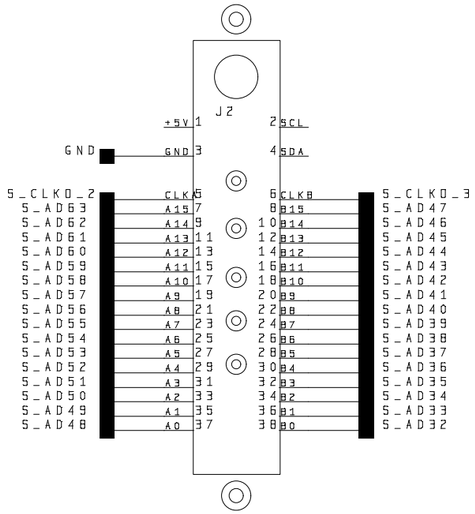

Mount 15uf cap close to VREG

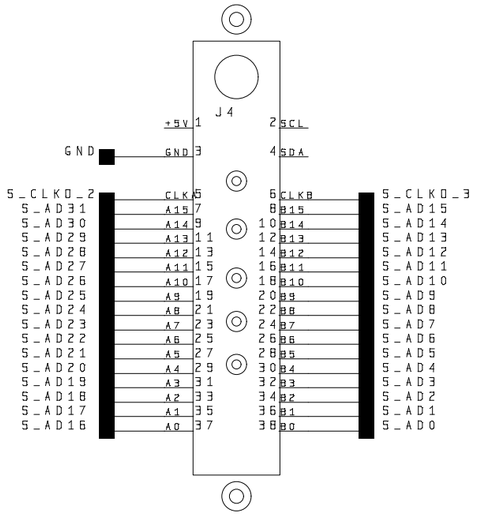
12-8-2000_14:08

12-8-2000_14:08

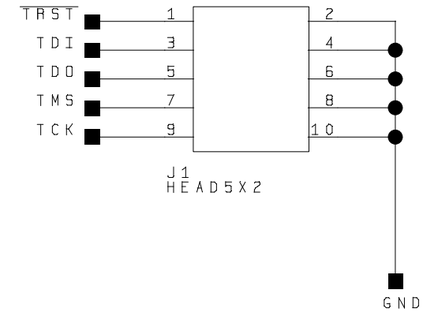
| | | | |
|---|---|---|---|
| ENG. GWRD | DATE | TITLE: DE1B555501 | |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER | REV 1.0 |

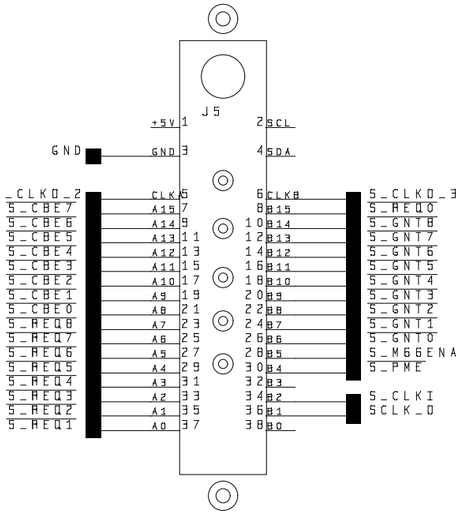
## Secondary AD Signals



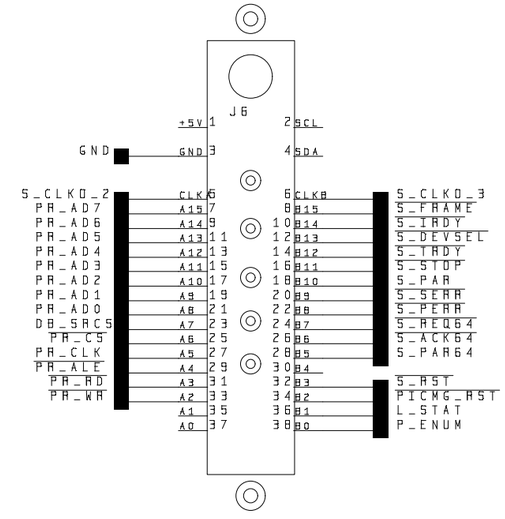




## JTAG Connections




## CBE, REQ, and GNT Lines




## ROM and Control Lines

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| | | | |
|---|---|---|---|
| ENG. GWRD | DATE | TITLE: DE1B55501 | |
| BOARD LOCATION: | | | |
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12-EB154-00

PCI_U_64

J102

PCI SLOT (Bottom - do not install)

-12V
TCK
S_INTC
S_INTA
PRSNT2_1
PRSNT2_2
RESERVED
KEYWAY
S_CLKO_C
S_REQ1
5VIO
S_AD31
S_AD29
+5V
S_AD27
S_AD25
S_CBE3
S_AD23
S_AD21
S_AD19
S_AD17
S_CBE2
S_IRDY
S_DEVSEL
S_LOCK
S_PERR
S_SERR
S_CBE1
S_AD14
S_AD12
S_AD10
S_M66ENA
S_AD8
S_AD7
+3V
S_AD5
S_AD3
S_AD1
5VIO
S_ACK64
GND
RESERVED
RESERVED

R1042 4.99K
R1113 4.99K

TRST
+12V
TMS
S_INTB
S_INTD
RESERVED
5VIO
RESERVED
S_R5T
5VIO
S_GNT1
S_PME
S_AD30
S_AD28
S_AD26
S_AD24
S_AD29
IDSEL
S_AD22
S_AD20
S_AD18
S_AD16
S_FRAME
S_IRDY
S_STOP
4.99K R112 5VIO
4.99K R110 5VIO
(Do not install resistors)
S_PAR
S_AD15
S_AD13
S_AD11
S_AD9
S_CBE0
S_AD6
S_AD4
S_AD2
S_AD0
5VIO
S_REQ64
+3V
+5V
S_CBE7
S_CBE5
5VIO
S_PAR64
S_AD62
S_AD60
S_AD58
S_AD56
S_AD54
5VIO
S_AD52
S_AD50
S_AD48
S_AD46
S_AD44
S_AD42
5VIO
S_AD40
S_AD38
S_AD36
S_AD34
S_AD32
RESERVED
RESERVED
GND

+5V
C38 .01UF
C39 .01UF
C41 .01UF
C43 .01UF
C51 0.1UF
Place Caps close to 12-39839 #0
GND

+5V
C44 .01UF
C45 .01UF
C46 .01UF
C49 .01UF
C50 0.1UF
Place Caps close to 12-39839 #1

15UF C53
+5V
GND

Mount 15uf Cap close to card edge

12-8-2000_14:08

| | | | |
|---|---|---|---|
| ENG. GWRD | DATE | TITLE: DE1B55501 | |
| BOARD LOCATION: | | | |
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| TDP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER | REV 12 |